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10/587,604	07/27/2006	Petrus Maria De Greef	NL040106US1	3561

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NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
MARTELLO, EDWARD	

ART UNIT	PAPER NUMBER
2628	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/587,604	DE GREEF, PETRUS MARIA	
	Examiner	Art Unit	
	Edward Martello	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the Appeal Brief filed on 18 March 2009, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/XIAO M. WU/

Supervisory Patent Examiner, Art Unit 2628

1. The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiefer et al. (European Patent Application Publication EP 0 875 882 A2, already of record, hereafter, '882).

3. Regarding claim 1, Schiefer teaches a display method comprising: generating images comprising source data (input video; '882; fig. 1 & 2; col. 10, ln. 14-26) and source frame (vertical) synchronization instants (IPVSYNC) having a source frame rate, storing the source data in a frame memory (memory, '882; fig. 3; col. 11, ln. 51-58; col. 18, ln. 13-39) under control of a first address pointer (write counter) having a start address being determined by the source frame synchronization instants (IPVSYNC) ('882; col. 13, ln. 13-39), reading during a read period display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants (DVSYNC) having a display frame rate ('882; col. 14, ln. 5-35), displaying the display data on a matrix display ('882; fig. 2) and controlling the source frame rate or the display frame rate to obtain, in a stable situation (display synchronizer; '882; col. 17, ln. 50-58, col. 18, ln. 1-10), the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during

the read period (‘882; col. 17, ln. 12-20; the pointers) and does not teach a ratio of two between the display frame rate and the source frame rate. Schiefer, however, teaches a ratio of four between the display frame rate and the source frame rate (“882; fig. 11-15, DCLK = 4*IPCLK, col. 21, ln. 15-20) and Schiefer does not limit the ratio to a factor of 4, as it can be a fractional multiple of the input video main clock (pixel rate) as may be desired and is shown in ‘882; col. 21, ln. 15-20. It would have been obvious to one of ordinary skill in the art at the time of the invention to have made the design choice of a ratio of two between the display frame rate and the source frame rate for the benefit of having a stable video display when the input image data rate is 1/2 half the screen refresh rate of the video display.

4. In regard to claim 2, Schiefer teaches a display system comprising: a video source for generating images comprising source data (input video; ‘882; fig. 1 & 2; col. 10, ln. 14-26) and source frame (vertical) synchronization instants (IPVSYNC), having a source frame rate, means for storing the source data in a frame memory (memory, ‘882; fig. 3; col. 11, ln. 51-58) under control of a first address pointer (write counter) having a start address being determined by the source frame synchronization instants (IPVSYNC) (‘882; col. 13, ln. 13-39); means for reading during a read period display data from the memory under control of a second address pointer (read counter) having a start address being determined by display frame synchronization instants (DVSYNC) having a display frame rate (‘882; col. 14, ln. 5-35), means for displaying the display data on a matrix display (‘882; fig. 2) and means for controlling the source frame rate or the display frame rate to obtain, in a stable situation (display synchronizer; ‘882; col. 17, ln. 50-58, col. 18, ln. 1-10), the first address pointer and the second address pointer starting with an offset in

time which has a fixed polarity during the read period (‘882; col. 17, ln. 12-20) and does not teach a ratio of two between the display frame rate and the source frame rate. Schiefer, however, teaches a ratio of four between the display frame rate and the source frame rate (“882; fig. 11-15, DCLK = 4*IPCLK, col. 21, ln. 15-20) and Schiefer does not limit the ratio to a factor of 4, as it can be a fractional multiple of the input video main clock (pixel rate) as may be desired and is shown in ‘882; col. 21, ln. 15-20. It would have been obvious to one of ordinary skill in the art at the time of the invention to have made the design choice of a ratio of two between the display frame rate and the source frame rate for the benefit of having a stable video display when the input image data rate is 1/2 half the screen refresh rate of the video display.

5. Regarding claim 3, Schiefer further teaches a display system wherein the means for controlling comprise: means for comparing the source frame synchronization instants (IPVSYNC) and the display synchronization instants (DVSYNC) or signals related thereto (‘882; fig. 13; col. 21, ln. 15-34), and means for adapting the source frame rate or the display frame rate in response to the comparing to obtain the second pointer always lagging (“882; fig. 13, DTGRUN signal) the first pointer during the read period in times or the other way around (‘882; fig. 13; col. 21, ln. 15-34).

6. Regarding claim 4, Schiefer further teaches a display system wherein the means for controlling comprise: means for determining the offset in time between one of the source frame synchronization instants (IPVSYNC) and one of the display frame synchronization instants (DVSYNC) succeeding each other(“882; col. 21, ln. 34-46), and means for adapting the source frame rate or the display frame rate to obtain a

substantially identical source frame rate and display frame rate ('882; col. 21, ln. 34-46); and a predetermined fixed value of the offset in time ('882; fig. 13, DTGRUN signal).

7. Regarding claim 5, Schiefer teaches a display system as claimed in claim 4 but does not teach wherein the means for adapting are arranged to obtain the offset in time between the first pointer and the second pointer being substantially equal to half a source write period, the source write period being the period in time required for the storing of the source data of one source frame of the source data. Schiefer teaches pre-filling the buffer memory to ensure that the display output can provide continuous horizontal active data regions ('882; col. 14, ln. 5-35). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the means for adapting are arranged to obtain the offset in time between the first pointer and the second pointer being substantially equal to half a source write period, the source write period being the period in time required for the storing of the source data of one source frame of the source data for the benefit of maintaining the optimum buffer fill to allow the most overrun and under run protection to handle short term variations is input video and output display timing that may occur in any system operating over a range of environmental conditions such a temperature, voltage, etc.

8. In regard to claim 6, Schiefer further teaches a display system as claimed in claim 2, wherein the means for displaying the display data further comprise: means for generating a clock signal (DCLK; '882; fig.7), and means for generating the display frame synchronization instants using the clock signal (DVSYNC; '882, fig. 10); and wherein the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal ('882; col. 15, ln. 29-37; col. 20, ln. 9-14).

9. Regarding claim 7 (Previously Presented), Schiefer further teaches a display system wherein the means for displaying the display data further comprise: means for generating a clock signal (DCLK; '882; fig.7), means for generating line instants indicating a start of the lines of the display data using the clock signal (DHSYNC; '882; fig. 9), the line instants (DHSYNC) determining line periods, and means for generating the display frame synchronization instants (DVSYNC) using the line instants (DHSYNC) ('882; col. 21, ln. 23-28), and wherein the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal to vary a duration of the line periods ('882; col. 15, ln. 29-37; col. 20, ln. 9-14).

10. In regard to claim 8 (Previously Presented), Schiefer further teaches a display system wherein the means for displaying the display data further comprise: means for generating a clock signal (DCLK; '882; fig.7), means for generating line instants indicating a start of the lines of the display data by counting the clock signal (DHSYNC; '882; fig. 9), the line instants determining line periods, and means for generating the display frame synchronization instants (DVSYNC) using the line instants ('882; col. 21, ln. 23-28), and wherein the means for controlling the display frame rate comprise means for adapting the line periods by varying a number of clock pulses of the clock signal to be counted ('882; col. 22, ln. 9-35).

11. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiefer et al. (European Patent Application Publication EP 0 875 882 A2, hereafter, '882) as applied to claims 1-8 above, and further in view of Chen et al. (U. S. Patent Application 2003/0164897 A1, hereafter '897).

12. Regarding claim 9, Schiefer teaches a display system method as claimed in claim 2 but does not teach wherein a display frame period has a duration being an inverse of the display frame rate and comprises the means for read period and an idle period, wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer, and wherein during the idle period no display data is read from the memory and wherein the means for controlling the display frame rate comprises means for varying the idle time. Chen, working in the same field of endeavor, however, teaches wherein a display frame period has a duration being an inverse of the display frame rate and comprises the means for read period and an idle period (current line delay), wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer (output x & y counters), and wherein during the idle period (current line delay) no display data is read from the memory (outputs blank lines) and wherein the means for controlling the display frame rate comprises means for varying the idle time ('897; fig. 7; ¶ 0124) for the benefit of synchronizing video image input and display image output frame rates without adjusting either the input or output video clock frequencies thereby simplifying overall clock circuit design and lowering cost. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Schiefer and Chen to produce a method that controls the output video idle period to synchronize the video output frame rate to the video input frame rate with the benefit of not adjusting either of the input or output video clock frequencies thus simplifying overall clock circuit design and lowering cost.

13. In regard to claim 10, Chen further teaches wherein the means for controlling comprise: means for determining the offset in time, and means for adapting the display frame rate to obtain a display frame rate being substantially identical to two times the source frame rate and to obtain a predetermined fixed offset in time, by having (i) the second pointer (output x & y counters) pointing to a first source video line of an already stored source video frame at an instant preceding the instant the first pointer (input x & y counters) is pointing to a first source video line a next source video frame to read the first source video line before the first source video line of the next source video frame is stored, and (ii) the second pointer (output x & y counters) pointing to a last source video line of the next source video frame at an instant later than an instant the first pointer (input x & y counters) is pointing to the last source video line of the next source video frame to read the last source video line of the next source video frame after it has been stored ('897; fig. 8-9, ¶ 0127-0128).

14. Regarding claim 11, Chen further teaches a display system wherein a display frame period has a duration being an inverse of the display frame rate and comprises the read period and an idle period, wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer (output x & y counters), and wherein during the idle period no display data is read from the memory (outputs blank lines) and wherein the means for controlling comprise: means for setting a free running display frame rate to a value lower than the value of the source display frame rate wherein a duration of the read period is shorter than a source frame period ('897; ¶ 0115), and means for restarting the display frame

periods in response to received source (input vertical) synchronization instants ('897; fig. 3, ¶ 0117).

Response to Arguments

15. Applicant's arguments, see page 5, filed 18 March 2009, with respect to the rejection(s) of claim(s) 1 and 2 under 35 USC 102 (b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Schiefer.

16. With respect to the rejection of claims 1 and 2, the applicant argues:

Independent claim I recites, in part, "A display method comprising, controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period and a ratio of two between the display frame rate and the source frame rate" (emphasis added). Independent claim 2 contains similar recitations.

As described in the specification in paragraph [0009], this subject matter relates to the use of a controller to control both the read and write address pointers in the memory in order to prevent video tearing. If the source and display frame rates are not equal, the controller adjusts both the frame rates and the address pointers so that, during the read period, one pointer does not cross the other, thus preventing tearing. *See* ¶ [0015]. This is highlighted by three features: (I) a time offset between the two address pointers, (2) a fixed polarity of the pointers during the read period, and (3) a constant ratio between the display frame rate and the source frame rate (here, the ratio is equal to 2). *See* ¶ [0054].

In contrast, Schiefer fails to disclose, teach, or suggest "controlling means for controlling the source frame rate or the display frame rate to obtain the address pointers, where the pointers start with a time offset, there is a fixed polarity between the pointers, and there is a ratio of two between the display and source frame rates," as recited in claim 1 and similarly recited in claim 2. The Examiner alleges that, because the write counter is initialized at the start of the frame and is used as a pointer with the reading delayed until the buffer is half full, Schiefer reads on the claims as written.

Appellant respectfully disagrees with this assertion. Schiefer discloses a timing generator for format conversion of video. *See* Abstract. This system reformats video by synchronizing the output and input rates and using a memory buffer to ensure smooth display. The memory write controller controls write

operations sequentially in a circular buffer sequence. *See* col. 13, ln. 34-39. The data path, once full, is then controlled by a timing controller.

The display synchronizer uses vertical and horizontal synchronization signals to force synchronization between the display timing generator and the video input signal. *See* col. 17, in. 53-57. The system supports multiple synchronization modes. *See* col. 18, ln. 7-10. Of greatest interest are the line synchronization and frame synchronization modes. *See* col. 20, in. 23 - col. 21, in. 46. In "Line Synch" mode, the display line rate is a function of the input video main clock. *See* col. 21, in. 15- 20. In "Frame Synch" mode, the input signal is locked to the output signal on a frame-by-frame basis. *See* col. 21, in. 34-36.

17. The Examiner respectfully disagrees with all but the times two ratio of the input versus output timing ratio in the Applicant's analysis above. To begin, the abstract of Schiefer provides a good overall view of the invention.

"This invention is directed to a method and apparatus for producing video signal timing for a display device that has a display format different from the input video format. It also provides a method and apparatus for producing video signal timing in cases where the input video line rate and display output line rates are not the same. Furthermore, a method and apparatus are provided for synchronizing the display output line rate to the input rate so that the source video line input rate can sustain the rate at which the input lines are processed to generate display video lines using a minimum amount of memory buffer for a variety of display processing methods. Another aspect of the present invention provides a method and apparatus for synchronizing display output timing to input video timing such that both are locked in terms of frame rate, but skewed in terms of frame phase, in order to accommodate latency incurred by processing of source video data to generate the display video data. A method and apparatus are also contemplated by this invention for adjusting the skew between the input source video frame timing and the display output video from timing to accommodate latency for various types of display processing such as, but not limited to, scaling, video format conversion, and filtering operations"

18. With this background established, please refer to figure 4 of Schiefer, which is a block diagram showing a memory write controller, a memory for buffering display data and a display timing controller for controlling the reading of display data out of the buffer

memory and passing it on to the display processor that outputs to the actual display device.

19. Schiefer teaches a write pointer into the buffer memory (actually two, if needed, so that interlaced formats can be easily changed to a progressive format; col. 12, ln. 35-52) and a read pointer to allow reading data out of the buffer memory for display. As the Applicant noted, Shafer starts writing into the buffer memory and waits until the buffer is sufficiently full depending on the input and output data rates **thus providing the fixed polarity offset between the pointers as required by claims 1 and 2** and the last cite in claims 1 and 2 ("882; fig. 11-15, DCLK = 4*IPCLK, col. 21, ln. 15-20) points to the detailed timing diagrams of the data buffering section of the invention where it is shown that the **output write clock is running at rate of four times the input clock rate** in the example given, providing a teaching of the last element in claims 1 and 2 of a factor of 4 instead of a factor of two. Schiefer does not does not limit the ratio to a factor of 4, as it can be a fractional multiple of the input video main clock (pixel rate) as stated in col. 21, ln. 15-20 so that it is not constrained to multiples of the horizontal line or image frame/field rates. As stated in the new grounds of rejection above, it would have been obvious to one of ordinary skill in the art at the time of the invention to have made the design choice of a ratio of two between the display frame rate and the source frame rate for the benefit of having a stable video display when the input image data rate is 1/2 half the screen refresh rate of the video display.

20. The applicant continues:

However, Schiefer discloses a half-line offset usually used in interlacing in order *to maintain a constant period. See* col. 17, ln. 12-20. The Schiefer application does not discuss the polarity of the pointers, nor does Schiefer

disclose using a fixed ratio between frame rates, as Schiefer's synchronization modes either synchronize frames based on a clock or synchronize frames so that they each have the substantially the same frame rate. This rate as disclosed in Schiefer is much Closer than the 2:1 ratio of frame rates recited in independent claims 1-2.

21. The Examiner respectfully disagrees with the Applicant's analysis above. Referring to figure 4 of Schiefer, there is provided a memory write controller, a memory for buffering display data and a display timing controller for controlling the reading of display data out of the buffer memory and passing it on to the display processor that outputs to the actual display device.

22. Schiefer teaches a write pointer into the buffer memory (actually two, if needed, so that interlaced formats can be easily changed to progressive format; col 12, ln. 35-52) and a read pointer to allow reading data out of the buffer memory. The ½ line offset noted above is for the case **locking of an interlaced format** (to provide the stable condition of the instant application) and is not intended to show only ½ line buffering and, as previously stated, Shafer starts writing into the image data buffer memory and waits until the buffer is sufficiently full depending on the input and output data rates **thus providing the fixed polarity offset between the pointers as required by claims 1 and 2** and the last cite in claims 1 and 2 ("882; fig. 11-15, DCLK = 4*IPCLK, col. 21, ln. 15-20) points to the detailed timing diagrams of the data buffering section of the invention where it is shown that the **output write clock is running at rate of four times the input clock rate** in the example given, providing a teaching of the last element in claims 1 and 2 of a factor of 4 instead of a factor of two. Schiefer does not does not limit the ratio to a factor of 4, as it can be a fractional multiple of the input video main clock (pixel rate) as

stated in col. 21, ln. 15-20 so that it is not constrained to multiples of the horizontal line or image frame/field rates. As stated in the new grounds of rejection above, it would have been obvious to one of ordinary skill in the art at the time of the invention to have made the design choice of a ratio of two between the display frame rate and the source frame rate for the benefit of having a stable video display when the input image data rate is 1/2 half the screen refresh rate of the video display.

23. With respect to the rejection of claims 3, 4, and 6-8 which depend on claim 2 and are therefore also rejected for at least the reasons stated above in connection with claim 2; they are rejected as well as for the separately rejected claimed subject matter recited therein as presented in section 9 above.

24. With respect to the rejection of claim 5, the applicant argues:

Dependent claim 5 recites, in part, "[a] display system as claimed in claim 4, wherein the means for adapting are arranged to obtain an offset in time between the first pointer and the second pointer being substantially equal to half a source write period..."

As described in the specification in paragraph [0054], this subject matter relates to the time between the address pointers. In this instance, the time offset is
the maximum distance between the pointers, as illustrated in Figs. 3 & 5C. As the two address pointers have the same polarity, the pointers have a minimum probability of crossing each other. This allows for a large difference in frame rates
(where one frame rate is substantially equal to twice the frame rate of the other) between the source and display, while still avoiding video tearing.

In contrast, Schiefer fails to disclose, teach or suggest "... an offset in time between the first pointer and the second pointer being substantially equal to half a source write period," as recited in claim 5. The Examiner alleges that, in view of Schiefer, it would have been obvious to maintain an average amount of data in the buffer to equally prevent an underflow or overwrite condition, which would be approximately half the buffer memory size.

Apellant disagrees with this assertion. A person of ordinary skill in the art would not have modified the invention of Schiefer to operate in the manner

recited in claim 5. An invention that otherwise might be viewed as an obvious modification of prior art will not be deemed obvious when a prior art reference teaches away from the invention. *McGinley v. Franklin Sports, Inc.,* 262 F.3d 1339, 1354 (Fed. Cir. 2000).

In the instant case, Schiefer discloses the use of half-line offset "to maintain a constant period between lock events" with regard to the source and output having substantially the same frame rates, where the choice of offset time is used to minimize timing errors. Col. 17, in. 17-20. A person of ordinary skill in the art would not modify Schiefer to achieve the subject matter recited in claim 5, however, as Schiefer discloses such use when the input and output have the same frame rate.

Instead, given a substantial difference in frame rates as recited in claim 5, a person of ordinary skill in the art applying the teachings of Schiefer would choose a point between the two frame rates that would give equal protection between overwrite and underflow conditions. Such a solution would be substantially different from the half-line offset recited in claim 5. As Schiefer would teach a person of ordinary skill in the art away from the subject matter recited in claim 5, Schiefer does not render claim 5 obvious.

25. The Examiner respectfully disagrees with the Applicant's analysis above.

Referring to figure 4 of Schiefer, there is provided a memory write controller, a memory for buffering display data and a display timing controller for controlling the reading of display data out of the buffer memory and passing it on to the display processor that outputs to the actual display device.

Schiefer teaches a write pointer into the buffer memory (actually two, if needed, so that interlaced formats can be easily changed to progressive format; col. 12, ln. 35-52) and a read pointer to allow reading data out of the buffer memory. The ½ line offset noted above is for the case **locking of an interlaced format** (to provide the stable condition of the instant application) and is not intended to show only ½ line buffering and, as previously stated, Shafer starts writing into the buffer memory and waits until the buffer is sufficiently full depending on the input and output data rates **thus providing the fixed**

polarity offset between the pointers as required by claim 5 and the last cite in claims 1 and 2 ("882; fig. 11-15, DCLK = 4*IPCLK, col. 21, ln. 15-20) points to the detailed timing diagrams of the data buffering section of the invention where it is shown that the **output write clock is running at rate of four times the input clock rate** in the example given, providing a teaching of the last element in claims 1 and 2 of a factor of 4 instead of a factor of two. Schiefer does not does not limit the ratio to a factor of 4, as it can be a fractional multiple of the input video main clock (pixel rate) as stated in col. 21, ln. 15-20 so that it is not constrained to multiples of the horizontal line or image frame/field rates. As stated in the new grounds of rejection above, it would have been obvious to one of ordinary skill in the art at the time of the invention to have made the design choice of a ratio of two between the display frame rate and the source frame rate for the benefit of having a stable video display when the input image data rate is 1/2 half the screen refresh rate of the video display.

26. With respect to the rejection of claims 9-11, the applicant argues:

Claims 9-11 depend on claim 2. Chen discloses a system to prevent buffer over/under-flow, with the input and output rate matching. *See* Abstract. Chen also discloses a display frame period being the inverse of the display frame rate and controlling the display frame rate by adjusting the idle time (time between read periods). Chen therefore fails to overcome the deficiencies of Schiefer described above in connection with the rejection of independent claim 2. Claims 9-11 are therefore patentable for at least the reasons stated above in connection with claim 2, as well as for the separately patentable subject matter recited therein.

27. The Examiner respectfully presents that Chen teaches the additional elements of claims 9-11 and that the remarks with respect to claim 2 upon which these claims depend

have been addressed above, therefore, claims 9-11 are properly rejected as presented in section 9 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Martello whose telephone number is (571) 270-1883. The examiner can normally be reached on M-F 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao Wu can be reached on (571) 272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EM/

Examiner, Art Unit 2628

/XIAO M. WU/
Supervisory Patent Examiner, Art Unit 2628